AMENDMENTS TO THE SPECIFICATION

Please replace the original title with the following amended title:

[[A]] MULTI-STAGE DELAY CLOCK GENERATOR

Please replace the paragraph [0013] with the following amended paragraph:

[0013] According to the claimed invention, the present invention provides a multi-stage delay clock generator comprising: a plurality of delay cells, each delay cell generating a delay signal to a subsequent delay cell in response to a delayed clock signal from a preceding delay cell and a delay control signal where a first delay cell among the plurality of delay cells receives an external clock signal, wherein each subsequent delay cell comprises a smaller delay step than the current delay cell; a phase detector, responsive to the external clock signal and a feedback clock signal, for generating a lock control signal; ~~an integrator, responsive to the lock control signal, for generating the delay control signal; and a control unit for programming the delay cells~~ and a control unit, responsive to the lock control signal, for generating the delay control signal for programming the delay cells.

Please replace the paragraph [0030] with the following amended paragraph:

[0030] Please refer to Fig. 5, which shows the ~~integrator~~ control unit 107 that uses fewer bits to save memory usage. The control unit 107 comprises a delay value counter 500 electrically coupled to the phase detector 106 to receive a lock control signal and outputs

a delay control signal to a plurality of multiplexers which are further electrically coupled to a plurality of latches, wherein each multiplexer is electrically coupled to one latch and forms a branch from the delay value counter 500 to each of the delay cell programming channel. The first branch from the delay value counter 500 electrically couples to the programming channel of the first delay cell via the multiplexer 520 and the latch 510. The multiplexer 520 selects from two inputs: a default value that is 0 and a first cell sel signal for the first delay cell and outputs a select signal to the latch. The latch 510 receives the select signal from the multiplexer 520 and then latches the delay value of which is sent to the first delay cell programming channel to program the first delay cell and sends a first lock value to the multiplexer of the next branch belonging to the subsequent delay cell. The first lock value sent by the latch 510 is used as the input value to the multiplexer 521. At the same time, the following delay cell value remains at the lowest bit. After the first delay lock determination is completed, the related register tunes the sensing window for the second delay cell programming channel 502. The programming bits are used repeatedly stage by stage until all the programming bits of all the delay cells are determined. The programmability of the present invention allows the use of only 1 set of delay counter controlling circuit so the complexity is greatly reduced.